IN THE CLAIMS

1. (Previously presented) A processor comprising:

classification circuitry operative to identify for each of a plurality of packets received in the processor a corresponding packet flow identifier;

control circuitry operatively coupled to the classification circuitry; and

at least one operational unit operatively coupled to the control circuitry;

wherein the control circuitry is operative to direct one or more packets having a given packet flow identifier to the at least one operational unit and maintains a desired function call sequencing over the one or more packets having the given packet flow identifier for one or more order-dependent processing tasks in the processor;

the control circuitry comprising ordering logic, the ordering logic comprising:

at least one ordering queue storing context identifiers in conjunction with respective function call identifiers and utilizing said context identifiers and said respective function call identifiers to maintain the desired function call sequencing for a designated set of functions; and

at least one configuration register storing information specifying said set of functions that are ordered by the at least one ordering queue.

2. (Original) The processor of claim 1 wherein the processor comprises a network processor configured to provide an interface for packet transfer between a network and a switch fabric.

3. (Original) The processor of claim 1 wherein the classification circuitry comprises at least one of a first pass classifier and a second pass classifier.

4. (Original) The processor of claim 1 wherein the control circuitry comprises at least one of a scheduler and queuing and dispatch logic.

5. (Original) The processor of claim 1 wherein the at least one operational unit comprises a plurality of computational units each having one or more execution engines associated therewith.

6. (Original) The processor of claim 1 wherein one or more of the packet flow identifiers each translates to a unique memory location in memory circuitry associated with the processor.

7. (Original) The processor of claim 6 wherein the unique memory location corresponding to a given packet flow identifier stores at least a counter specifying a number of functions performed for an associated packet flow.

8. (Original) The processor of claim 1 wherein the control circuitry is operative to determine if more than one function associated with a particular order-dependent processing task is being performed on multiple packets having the same packet flow identifier during a particular processing interval.

9. (Original) The processor of claim 8 wherein if more than one function associated with a particular order-dependent processing task is being performed on multiple packets having the same packet flow identifier during a particular processing interval, the control circuitry maintains the desired function call sequencing for the particular order-dependent processing task.

10. (Original) The processor of claim 8 wherein if more than one function associated with a particular order-dependent processing task is not being performed on multiple packets having the same packet flow identifier during a particular processing interval, the control circuitry permits an arbitrary function call sequencing for the particular order-dependent processing task.

11. (Original) The processor of claim 1 wherein the packet flow identifier for the given packet is extracted from a header of the packet.

12. (Original) The processor of claim 1 wherein each of the received packets has a context identifier assigned thereto within the processor prior to function call issuance for that packet.

13. (Original) The processor of claim 12 wherein the context identifiers are selected from a fixed number of tokens.

14. (Original) The processor of claim 13 wherein the fixed number of tokens comprises approximately 256 tokens, the context identifier comprising an 8-bit identifier.

15. (Original) The processor of claim 12 wherein a given set of packets having the same packet flow identifier have different context identifiers assigned thereto.

16. (Original) The processor of claim 12 wherein the context identifiers assigned to the received packets are utilized to maintain the desired function call sequencing for the received packets associated with a particular packet flow identifier.

17. (Original) The processor of claim 1 wherein the processor is configured as an integrated circuit.

18. (Currently amended) A method for use in processing packets in a processor, the method comprising the steps of:

identifying, in classification circuitry, for each of a plurality of packets received in the processor a corresponding packet flow identifier; and

directing, in control circuitry, one or more packets having a given packet flow identifier to at least one operational unit of the processor and ~~maintains~~ maintaining a desired function call sequencing over the one or more packets having the given packet flow identifier for one or more order-dependent processing tasks in the processor;

wherein at least one ordering queue, in the control circuitry, stores context identifiers in conjunction with respective function call identifiers and ~~utilizing~~ utilizes said

context identifiers and said respective function call identifiers to maintain the desired function call sequencing for a ~~desired~~ designated set of functions; and

at least one configuration register, in the control circuitry, stores information specifying said set of functions that are ordered by the at least one ordering queue.